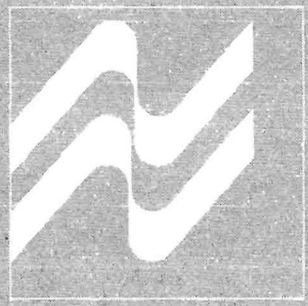


SECTION 10
KEYBOARD ENCODER CIRCUITS

Keyboard Encoder Circuits

For additional application information, see AN-128 and AN-139 at the end of this section.

MM5740 90-key keyboard encoder

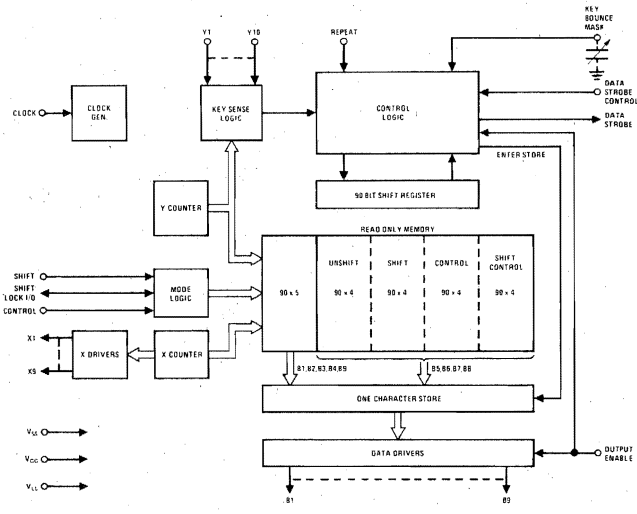
general description

The MM5740 MOS/LSI keyboard encoder is a complete keyboard interface system capable of encoding 90 single pole single throw switch closures into a usable 9-bit code. It is organized as a bit paired system and is capable of N key or two key rollover. The MM5740 is fabricated with silicon gate technology and provides for direct TTL/DTL compatibility on Data and Strobe outputs without the use of any special interface components.

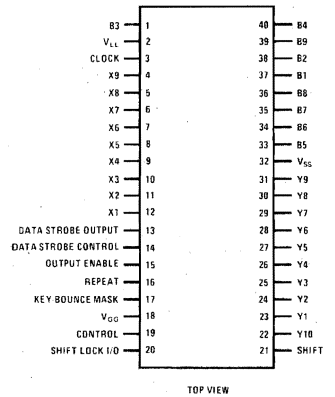
features

- TRI-STATE® data outputs directly compatible with TTL/DTL or MOS logic
- Function inputs directly compatible with TTL/DTL logic
- Only one TTL level clock required
- N key/two key rollover (mask programmable)
- 90 key-quad mode capability
- One character data storage
- Repeat function (selectable)
- Shift lock with indicator capability
- Key bounce masking by single external capacitor
- Level or pulse data strobe output
- Data strobe pulse width control

block and connection diagrams



Dual-In-Line Package



TOP VIEW

Order Number MM5740N
See Package 24

TRI-STATE is a registered trademark of National Semiconductor Corp.

absolute maximum ratings

Data and Clock Input Voltages and Supply Voltages with Respect to V_{SS}	+0.3V to −20V
Power Dissipation	600 mW at T_A = +25°C
Operating Temperature	−25°C to +70°C ambient
Storage Temperature	−65°C to +160°C
Lead Temperature (Soldering, 10 seconds)	300°C

electrical characteristics (Note 1,5)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Clock Repetition Rate		10		200	kHz
Clock Pulse Width	Rep. Rate = 200 kHz	2.4		2.6	μs
	Rep. Rate = 10 kHz	20		80	μs
Clock Amplitude					
Logic Level "0"				3.25	V
Logic Level "1"		+0.4			V
Clock Transition Times					
Risetime	Rep. Rate = 200 kHz			100	ns
Falltime	Rep. Rate = 200 kHz			100	ns
Clock Input Capacitance			5.0		pF
Data Input Levels, Y1 thru Y10					
Logic Level "0"				V_{SS} − 1.5	V
Logic Level "1"		−4.5			V
Logic Level "0"				3.25	V
Logic Level "1"		+0.4			V
Data Strobe Control					
Logic Level "0"				+3.5	V
Logic Level "1"		+0.4			V
Data Output Levels, X1 thru X9					
Logic Level "0"	When Connected to Y1 thru Y10			V_{SS} − 0.75	V
Logic Level "1"	via Switch Matrix, (C_L = 75 pF)	−4.5			V
B1 thru B9 and Data Strobe					
Logic Level "0"	I = 100μA (Note 2)			V_{SS} − 1.0	V
Logic Level "1"	I = 1.6 mA (Note 2)	+0.4			V
Shift Lock Voltage Open	Before Closure		V_{GG} − 2.0		V
Shift Lock Voltage Closed	Switch Closed		V_{SS}		V
Shift Lock Voltage Locked	After Release, (I = 1.0 mA) (Figure 2)		V_{SS} − 5.0	V_{SS} − 8.0	V
Transition Times					
Data Strobe (T_{DS1})	C_L = 100 pF, I = 1.6 mA			2.5	μs
Data Strobe (T_{DS0})	C_L = 100 pF, I = 100μA			1.0	μs
Data Output Levels					
(T_{DO1})	C_L = 100 pF, I = 1.6 mA			2.5	μs
(T_{DO0})	C_L = 100 pF, I = 100μA			1.0	μs
Output Enable Setup Time (T_{OES})		2.5			μs
Output Enable Release Time (T_{OER})		2.5			μs
Repeat Input Pulse Width (T_{RPW})	(Note 3)				
	f_{CLOCK} = 10 kHz	10			ms
	f_{CLOCK} = 200 kHz	0.5			ms
Power Supply Current	I_{GG}, I_{SS}		20	35	mA

Note 1: These specifications apply for V_{SS} = +5.0 VDC ±5%, V_{GG} = −12.0 VDC ±5%, V_{LL} = GND and T_A = 0°C to +70°C.

Note 2: When outputs B1 thru B9 and Data Strobe are driving TTL/DTL $V_{SS} - V_{LL} \leq 5.25V$. When driving MOS, $V_{SS} - V_{LL} \leq 10.0V$.

Note 3: $T_{RPW\ min.} = 100 \times \frac{1}{f_{clock}}$

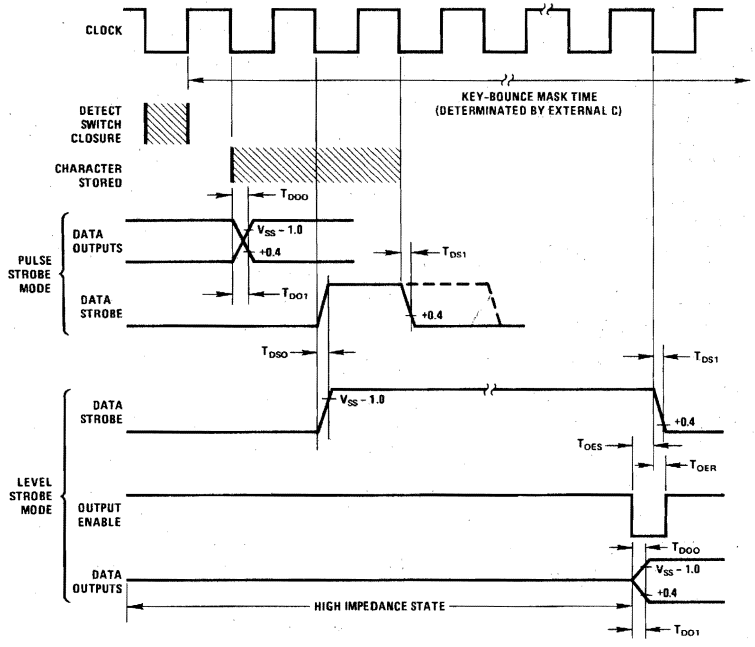
Note 4: If shift and control inputs are derived from a single pole, single throw switch closure to V_{SS}, a 100 OHM resistor returned to V_{LL} (GND) is required on these inputs.

Note 5: The following inputs have internal pull-up resistors to V_{SS}: clock, output enable, repeat, shift, control.

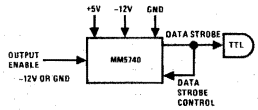
description of pin functions

NAME	PIN NO.	FUNCTION
X1-X9	4-12	These pins are chip outputs which are used to drive the key switch matrix. When activated (at the appropriate scan time) they are driven high.
Y1-Y10	22-31	Pins 22-31 are the Y sense inputs which are connected to the X drive lines via the key switch matrix. They are internally precharged to a low state and are pulled high upon switch closure.
B1-B9	1, 33-40	These are the data outputs which represent the code for each keyswitch. They are TRI-STATE outputs with direct TTL compatibility. When the output enable input (Pin 15) is high, these outputs are in the third state.
Data Strobe Output	13	The function of this pin is to indicate that valid data has been entered by the keyboard and is ready for acceptance. An active data strobe is indicated by a high level. The data strobe may be operated in the pulse or level mode as indicated by the timing diagram.
Data Strobe Control	14	The basic purpose of this input is to provide data strobe output pulse width control. When connected to the data strobe output (Pin 13), the data strobe will exhibit a one bit wide pulse width. The pulse width may be varied by interposing an RC network between the data strobe output and the strobe control input. For level mode of operation the data strobe control input may be tied to V_{SS} or to the data strobe output.
Output Enable	15	This input serves to TRI-STATE the data output (B1-B9) lines. In addition, it controls the return of the data strobe to the idle condition (low state) which is needed in the level strobe mode of operation.
Repeat	16	The repeat input is designed to accept a repeat signal via the repeat key. One data strobe will be issued for each positive interval of the repeat signal. Thus, if a 10 Hz signal is applied to the repeat input via the repeat switch, a 10 character per second data strobe will be issued when a data key and the repeat key are held depressed.
Key-Bounce Mask	17	This pin is intended as a timing node to mask switch key-bounce. The mask time interval is generated by connecting a capacitor to this pin.
Shift	21	When this input is brought to a logic "0" (V_{SS}) level, the encoder will assume the shifted character mode.
Control	19	A logic "0" places the encoder in the control character mode.
Shift Lock I/O	20	This pin is intended to serve as an input when the shift lock key is depressed. It places the encoder in the shift mode. Upon release of the key, the shift mode will be maintained and this pin will serve as an output to drive an indicator. This function is reset by depressing the shift key.
Clock	3	A TTL compatible clock signal is applied to this pin. A bit time is defined as the time from one negative going transition to the succeeding negative going transition of the clock.
V_{SS}	32	+5.0V supply
V_{LL}	2	Ground
V_{GG}	18	-12V supply

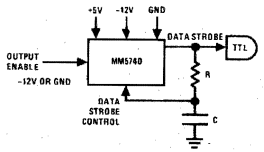
timing diagram



applications information

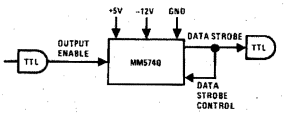


A) DATA STROBE PULSE WIDTH = ONE CLOCK PERIOD



B) WIDER DATA STROBE PULSE WIDTH CONTROLLED BY RC

Pulse Data Strobe Mode



Level Data Strobe Mode

key bounce capacitor values

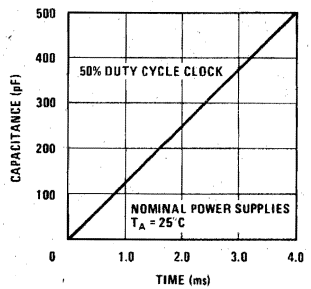


FIGURE 1. Key-Bounce Mask Time

application

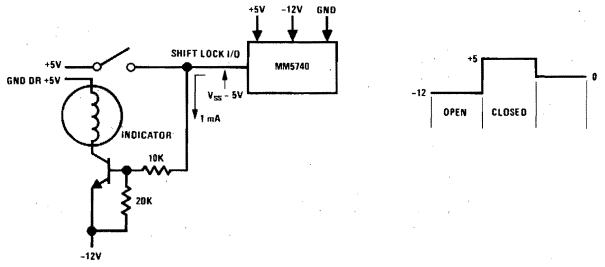
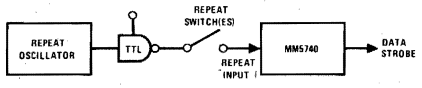
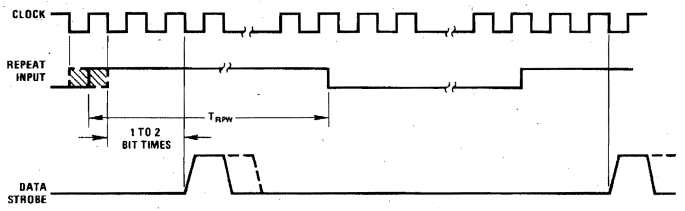


FIGURE 2. Shift Logic I/O Interface

repeat switch function



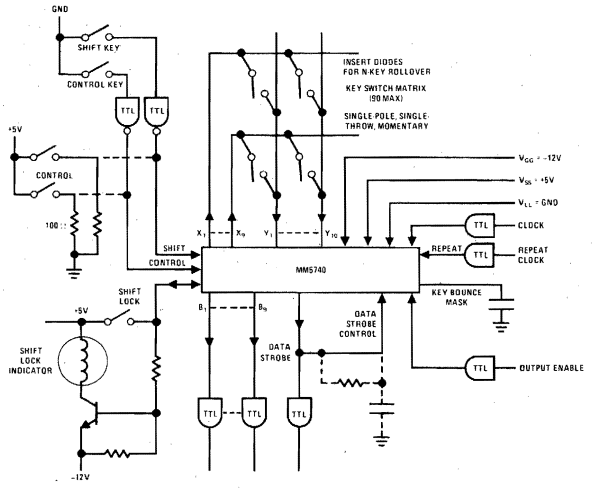
Repeat Switch Connections



Note: Both Repeat Switch and a Data Key must be depressed to enable repeat function. For N-Key Rollover, the data outputs will represent the current valid data key (N Key Roll during Repeat).

Repeat Function

typical applications



CODE ASSIGNMENT CHART

Customer: _____

Date: _____

MATRIX ADDRESS		COMMON					UNSHIFT				SHIFT				CONTROL				SHIFT CONTROL				CHARACTER			
X	Y	B_1	B_2	B_3	B_4	B_9	B_5	B_6	B_7	B_8	B_5	B_6	B_7	B_8	B_5	B_6	B_7	B_8	B_5	B_6	B_7	B_8	US	S	C	SC
(Note 3)	1																									
	2																									
	3																									
	4																									
	5																									
	6																									
	7																									
	8																									
	9																									
	10																									
	1																									
	2																									
	3																									
	4																									
	5																									
	6																									
	7																									
	8																									
	9																									
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	1																									
	2																									
	3																									
	4																									
	5																									
	6																									
	7																									
	8																									
	9																									
	10																									

☐ N-Key Rollover

☐ 2 Key Rollover

Page ☐ of 3 (Note 1)

Note: Use B8 if parity bit is desired

Note 1: 3 code assignment charts are required for each keyboard encoder pattern. Fill in a "1" or "0" in each output box (B_1 thru B_9). Indicate page number.

Note 2: The matrix is 9 "X" locations by 10 "Y" locations.

Note 3: Write in 10 one's, 10 two's, etc. in successive X address locations up to 9. This will fill 3 charts. The first page will have address matrix location 1,1; 1,2: 1,3... 1,10; 2,1; 2,2... 2,10; 3,1, etc. up to 3,10. Page 2 has 4,1 to 6,10. Page 3 has 7,1 to 9,10.

Note 4: A contact closure at the address matrix location will cause the appropriate bit pattern to appear at the output in negative true logic. V_{OH} = "0"; V_{OL} = "1."

Note 5: See application note AN-80 for coding example.

MM5740AAE, MM5740AAF CODE ASSIGNMENT CHARTS

MATRIX ADDRESS		COMMON					UNSHIFT				SHIFT				CONTROL				SHIFT CONTROL				CHARACTER			
X	Y	B_1	B_2	B_3	B_4	B_9	B_5	B_6	B_7	B_8	B_5	B_6	B_7	B_8	B_5	B_6	B_7	B_8	B_5	B_6	B_7	B_8	US	S	C	SC
1	1	0	0	0	1	0	1	1	0	1	1	1	0	1	1	1	0	1	1	1	0	1	8	8	8	8
1	2	0	0	1	0	0	1	1	0	1	1	1	0	1	1	1	0	1	1	1	0	1	4	4	4	4
1	3	1	0	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	5	5	5	5
1	4	1	0	0	0	0	1	1	0	1	1	1	0	1	1	1	0	1	1	1	0	1	1	1	1	1
1	5	0	1	0	0	0	1	1	0	1	1	1	0	1	1	1	0	1	1	1	0	1	2	2	2	2
1	6	1	1	0	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	3	3	3	3
1	7	0	0	0	0	1	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	☺	☺	☺	☺
1	8	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	6	6	6	6
1	9	1	0	0	1	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	9	9	9	9
1	10	1	1	1	0	0	1	1	0	1	1	1	0	1	1	1	0	1	1	1	0	1	7	7	7	7
2	1	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	FF	FF	FF	FF
2	2	1	0	1	1	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	CR	CR	CR	CR
2	3	0	0	1	1	0	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	FS	FS	FS	FS
2	4	1	0	1	1	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	GS	GS	GS	GS
2	5	1	1	0	1	0	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	VT	VT	VT	VT
2	6	0	1	1	1	0	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	SO	SO	SO	SO
2	7	0	0	0	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	SP	SP	SP	SP
2	8	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	HT	HT	HT	HT
2	9	0	0	0	1	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	BS	BS	BS	BS
2	10	1	0	1	1	1	0	1	0	0	1	1	0	1	0	1	0	0	1	1	0	1				
3	1	0	0	0	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	☺	☺	☺	☺
3	2	0	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	LF	LF	LF	LF
3	3	0	0	0	0	0	1	0	1	0	0	0	1	1	1	0	0	1	0	0	0	0	P	@	DLE	NUL
3	4	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	DEL	DEL	DEL	DEL
3	5	1	1	0	1	0	1	1	0	1	0	1	0	0	1	1	0	1	0	1	0	0	:	:	:	:
3	6	0	1	1	1	1	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	.	.	.	.
3	7	1	1	1	1	0	0	1	0	1	1	1	0	0	0	1	0	1	1	1	0	0		?		?
3	8	0	0	0	0	0	1	0	1	0	1	0	1	0	1	0	0	1	1	0	0	1	P	P	DLE	DLE
3	9	1	1	1	1	0	0	0	1	1	0	0	1	1	0	0	0	0	0	0	0	0	0	0	SI	SI
3	10	0	1	0	1	1	1	1	0	0	0	1	0	1	1	1	0	0	0	1	0	1	:	:	:	:

MATRIX ADDRESS		COMMON					UNSHIFT				SHIFT				CONTROL				SHIFT CONTROL				CHARACTER			
X	Y	B_1	B_2	B_3	B_4	B_9	B_5	B_6	B_7	B_8	B_5	B_6	B_7	B_8	B_5	B_6	B_7	B_8	B_5	B_6	B_7	B_8	US	S	C	SC
4	1	1	0	0	1	0	1	1	0	0	0	1	0	1	1	1	0	0	0	1	0	1	9	)	9	)
4	2	1	0	0	1	0	0	0	1	1	0	0	1	1	0	0	0	0	0	0	0	0	I	I	HT	HT
4	3	1	1	1	1	1	0	0	1	1	1	0	1	0	0	0	0	0	1	0	0	1	O	_	SI	US
4	4	1	1	0	1	0	0	0	1	0	1	0	1	1	0	0	0	1	1	0	0	0	K	[	VT	ESC
4	5	0	0	1	1	0	0	0	1	1	1	0	1	0	0	0	0	0	1	0	0	1	L	\	FF	FS
4	6	0	0	1	1	0	0	1	0	1	1	1	0	0	0	1	0	1	1	1	0	0	,	←	,	←
4	7	0	1	1	1	1	0	1	0	0	1	1	0	1	0	1	0	0	1	1	0	1	-	→	-	→
4	8	0	0	1	1	0	0	0	1	1	0	0	1	1	0	0	0	0	0	0	0	0	L	L	FF	FF
4	9	1	1	0	1	0	0	0	1	0	0	0	1	0	0	0	0	1	0	0	0	1	K	K	VT	VT
4	10	0	0	0	1	0	1	1	0	1	0	1	0	0	1	1	0	1	0	1	0	0	8	(	8	(
5	1	0	1	1	0	0	1	1	0	0	0	1	0	1	1	1	0	0	0	1	0	1	G	&	G	&
5	2	1	0	1	0	0	1	0	1	0	1	0	1	0	1	0	0	1	1	0	0	1	U	U	NAK	NAK
5	3	1	0	0	1	0	1	0	1	0	1	0	1	0	1	0	0	1	1	0	0	1	Y	Y	EM	EM
5	4	0	1	0	1	0	0	0	1	1	0	0	1	1	0	0	0	0	0	0	0	0	J	J	LF	LF
5	5	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	0	1	0	0	0	1	H	H	BS	BS
5	6	1	0	1	1	0	0	0	1	0	1	0	1	1	0	0	0	1	1	0	0	0	M	J	CR	GS
5	7	0	1	1	1	1	0	0	1	0	1	0	1	1	0	0	0	1	1	0	0	0	N	^	SO	RS
5	8	1	0	1	1	0	0	0	1	0	0	0	1	0	0	0	0	1	0	0	0	1	M	M	CR	CR
5	9	0	1	1	1	0	0	0	1	0	0	0	1	0	0	0	0	1	0	0	0	1	N	N	SO	SO
5	10	1	1	1	0	0	1	1	0	1	0	1	0	0	1	1	0	1	0	1	0	0	7	'	7	'
6	1	1	0	1	0	0	1	1	0	0	0	1	0	1	1	1	0	0	0	1	0	1	5	%	5	%
6	2	0	1	0	0	0	1	0	1	1	1	0	1	1	1	0	0	0	1	0	0	0	R	R	DC2	DC2
6	3	0	0	1	0	0	1	0	1	1	1	0	1	1	1	0	0	0	1	0	0	0	T	T	DC4	DC4
6	4	0	1	1	0	0	0	0	1	1	0	0	1	1	0	0	0	0	0	0	0	0	F	F	ACK	ACK
6	5	1	1	1	0	0	0	0	1	0	0	0	1	0	0	0	0	1	0	0	0	1	G	G	BEL	BEL
6	6	0	1	1	0	0	1	0	1	0	1	0	1	0	1	0	0	0	1	0	0	0	V	V	SYN	SYN
6	7	0	1	0	0	0	0	0	1	0	0	0	1	0	0	0	0	1	0	0	0	1	B	B	STX	STX
6	8	0	0	0	1	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	CAN	CAN	CAN	CAN
6	9	1	0	0	1	0	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	EM	EM	EM	EM
6	10	0	0	1	0	0	1	1	0	1	0	1	0	0	1	1	0	1	0	1	0	0	4	S	4	S

Negative True Logic

$B_1 - B_7$ = ASCII Code
B_8 = Even parity (on $B_1, B_2, B_3, B_4, B_5, B_6, B_7, B_8$)
B_9 = Selective Repeat Bit

Note: Use B_8 if parity bit is desired.

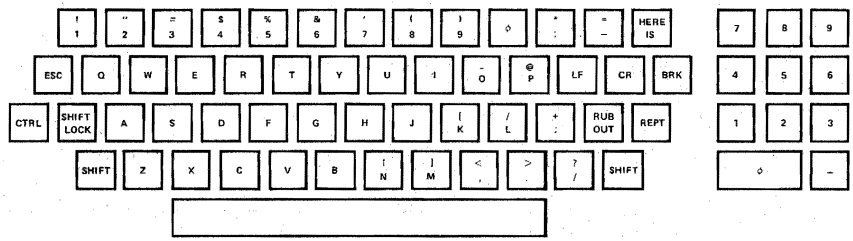
MM5740AAE, MM5740AAF CODE ASSIGNMENT CHARTS (CONTINUED)

MATRIX ADDRESS		COMMON					UNSHIFT				SHIFT				CONTROL				SHIFT CONTROL				CHARACTER			
X	Y	B_1	B_2	B_3	B_4	B_9	B_5	B_6	B_7	B_8	B_5	B_6	B_7	B_8	B_5	B_6	B_7	B_8	B_5	B_6	B_7	B_8	US	S	C	SC
7	1	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	DC2	DC2	DC2	DC2
7	2	1	0	1	0	0	0	0	1	1	0	0	1	1	0	0	0	0	0	0	0	0	E	E	ENG	ENG
7	3	1	1	0	0	0	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	DC3	DC3	DC3	DC3
7	4	0	0	1	0	0	0	0	1	0	0	0	1	0	0	0	0	1	0	0	0	1	D	D	EOT	EOT
7	5	0	0	1	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	DC4	DC4	DC4	DC4
7	6	1	1	0	0	0	0	0	1	1	0	0	1	1	0	0	0	0	0	0	0	0	C	C	ETX	ETX
7	7	1	0	1	0	0	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	NAK	NAK	NAK	NAK
7	8	0	1	1	0	0	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	SYN	SYN	SYN	SYN
7	9	1	1	1	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	ETB	ETB	ETB	ETB
7	10	1	1	0	0	0	1	1	0	0	0	1	0	1	1	1	0	0	0	1	0	1	3	#	3	#
8	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	ENQ	ENQ	ENQ	ENQ
8	2	1	1	1	0	0	1	0	1	1	1	0	1	1	1	0	0	0	1	0	0	0	W	W	ETB	ETB
8	3	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	ACK	ACK	ACK	ACK
8	4	1	1	0	0	0	1	0	1	0	1	0	1	0	1	0	0	1	1	0	0	1	S	S	DC3	DC3
8	5	1	1	1	0	0	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	BEL	BEL	BEL	BEL
8	6	0	0	0	1	0	1	0	1	1	1	0	1	1	1	0	0	0	1	0	0	0	X	X	CAN	CAN
8	7	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	SI	SI	SI	SI
8	8	0	0	0	0	0	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	DLE	DLE	DLE	DLE
8	9	1	0	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	DC1	DC1	DC1	DC1
8	10	0	1	0	0	0	1	1	0	1	0	1	0	0	1	1	0	1	0	1	0	0	2	"	2	"
9	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	NUL	NUL	NUL	NUL
9	2	1	0	0	0	0	1	0	1	1	1	0	1	1	1	0	0	0	1	0	0	0	Q	Q	DC1	DC1
9	3	1	1	0	1	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	ESC	ESC	ESC	ESC
9	4	1	0	0	0	0	0	0	1	0	0	0	1	0	0	0	0	1	0	0	0	1	A	A	SOH	SOH
9	5	1	0	0	0	0	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	SOH	SOH	SOH	SOH
9	6	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	0	1	1	0	0	1	Z	Z	SUB	SUB
9	7	0	1	0	0	0	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	STX	STX	STX	STX
9	8	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	ETX	ETX	ETX	ETX
9	9	0	0	1	0	0	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	EOT	EOT	EOT	EOT
9	10	1	0	0	0	0	1	1	0	1	0	1	0	0	1	1	0	1	0	1	0	0				

Negative True Logic

$B_1 - B_7$ = ASCII Code
B_8 = Even parity (on B_1, B_2, B_3, B_4, B_5, B_6, B_7, B_8)
B_9 = Selective Repeat Bit

Note: Use B_8 if parity bit is desired.



ASR

ASR 33
MM5740AAE (N-KEY ROLLOVER)
MM5740AAF (2-KEY ROLLOVER)

Typical Keyboard Arrangement

Keyboard Encoder Circuits

MM5745, MM5746 78-key keyboard encoder

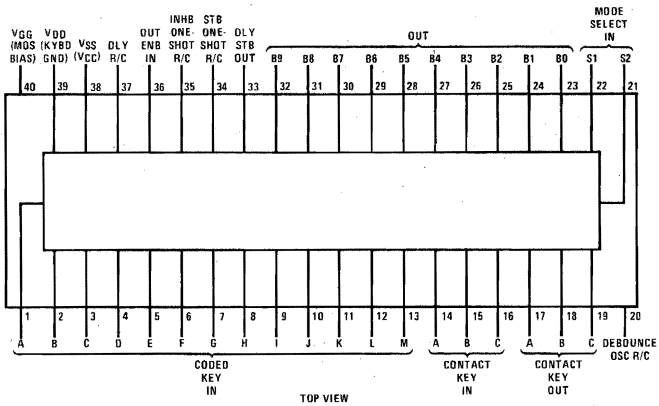
general description

The MM5745, MM5746 MOS/LSI keyboard encoder is a complete keyboard interface system capable of encoding 78 double-pole single-throw switches (hall-effect, capacitive, or contact) into a 10-bit code. Full quad-mode operation allows 4 independent 10-bit codes per switch. Debounce circuits for contact keys are provided for 3 function switches. The MM5745, MM5746 is fabricated with low threshold metal gate P-channel enhancement devices and ion-implanted resistors and provides for direct TTL/DTL compatibility on Data and Strobe outputs without the use of any special interface components.

features

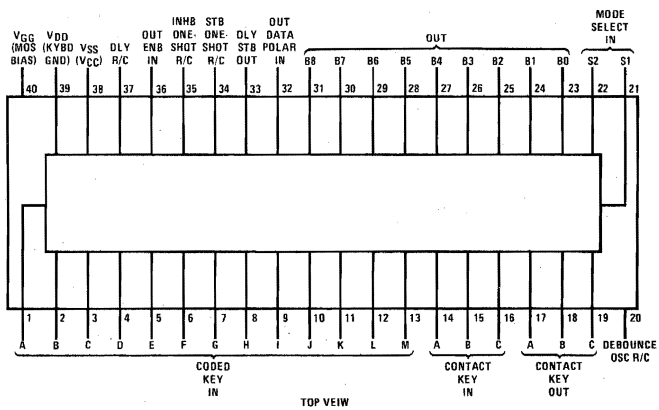
- 78- key quad-mode capability
- N-key/2-key rollover
- 1 character data storage
- Level or pulse data strobe output
- Data strobe pulse width control
- Key bounce delay control
- Function key debounce circuits
- Data and Strobe outputs directly compatible with TTL/DTL or MOS logic

connection diagrams (Dual-In-Line Packages)



TOP VIEW

Order Number MM5745N
See Package 24



TOP VEIW

Order Number MM5746N
See Package 24

absolute maximum ratings

Voltage at Any Pin Except Outputs	V_{SS} + 0.3V to V_{SS} − 25V
Voltage at Any Output Pin	V_{SS} + 0.3V to V_{SS} − 20V
Power Dissipation	700 mW at T_A = 25°C
Operating Temperature	−25°C to +70°C ambient
Storage Temperature	−65°C to +160°C
Lead Temperature (Soldering, 10 seconds)	300°C

electrical characteristics (Note 1)

	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{IH}	High Level Input Voltage	With Respect to V_{SS}			−1.5	V
V_{IL}	Low Level Input Voltage	With Respect to V_{DD}			0.8	V
V_{OH}	High Level Output Voltage	With Respect to V_{SS}			−1.8	V
V_{OL}	Low Level Output Voltage	With Respect to V_{DD}, I_{OL} = 1.6 mA			0.4	V
I_{IL}	Low Level Input Current (Logic)	V_{SS} = 5.25V, V_{IN} = 0.4V (Not Including MOS Inputs), (Note 2)			−1.6	mA
t_r	10–90% Output Rise Time	C_L = 50 pF			1	μs
t_f	90–10% Output Fall Time	C_L = 50 pF			1	μs
t_d	Delay Time Input to Output	Delay Capacitor = 0, R_L = 200Ω			20	μs
t_s	Delay from Strobe to Data Output		0.5			μs
D_{td}	Delay R/C Time Delay	±25% Variation Max per Given Set of R and C	40		80	μs
		R—Useful Range	200		680	kΩ
		C—Useful Range at Min R	0.001		0.002	μFd
I_{td}	Inhibit One-Shot Time Delay	±25% Variation Max per Given Set of R and C	1		30	ms
		R—Useful Range	200		680	kΩ
		C—Useful Range at Min R	0.025		0.75	μFd
S_{td}	Strobe One-Shot Time Delay	±25% Variation Max per Given Set of R and C Typ	40		80	μs
		R—Useful Range	200		680	kΩ
		C—Useful Range at Min R	0.001		0.002	μFd
B_{td}	Debounce Oscillator	±25% Variation Max per Given Set of R and C	1		7	ms
		R—Useful Range	200		680	kΩ
		C—Useful Range at Min R	0.025		0.175	μFd
I_{SS}	Supply Current	V_{SS} = 5.25V			100	mA
I_{GG}	Bias Current	V_{GG} = −18V			5	mA

Note 1: V_{SS} = 5V ±5%, V_{DD} = Gnd, V_{SS} = −12V to −18V and T_A = 0°C to +70°C.
Note 2: The following inputs have internal pull-up resistors to V_{SS}: Output Enable, Output Data Polarity.

functional description

A block diagram of the MM5745 and MM5746 keyboard encoders is shown in *Figure 1*. Connection diagrams for these devices are shown on the previous page. The following discussions are based on *Figure 1*.

Coded Key Inputs

Thirteen MOS type coded key inputs, designated A–M can be coded in an M of N format. These codes must be specified with each reprogramming of the coding mask. A maximum of 78 input codes may be specified. Typically, coding takes the form of 2 out of 13 inputs.

Contact Key Inputs

Three MOS type contact key inputs designated A, B and C can be used to debounce contact type switches.

functional description (Continued)

Mode Select Inputs

Two mode inputs, designated S1 and S2, are used to select any 1 of the 4 output coding modes. The binary number selections to represent a given output code mode must be specified with each reprogramming of the coding mask.

Output Data Polarity Input (MM5746 Only)

The Output Data Polarity Input, when switched from one state to the other, causes a reversal of the output data polarity. When open, the input is held high, logical "1", by an internal pull-up resistor, and the data comes through non-inverted from the output ROM.

Output Enable Input

The Output Enable Input enables the output storage latches to accept new output data and allows an output strobe to be generated. When the input is open, an internal pull-up resistor holds the input high, logical "1", and enables the output. When held low, logical "0", the output and strobe are disabled.

Debounce Oscillator R/C Input

The Debounce Oscillator R/C Input is a timing input that can eliminate closing or opening contact bounce durations of between 1 to 2 clock periods. Depending upon the length of bounce and R/C values chosen, the output will be delayed from the inputs from 1 to 14 ms. The resistor connects to V_{GG} and the Capacitor connects to V_{SS}.

Strobe One-Shot R/C Input

The Strobe One-Shot R/C Input is a timing input used to adjust the width of the delayed output strobe. The strobe width has a ±25% variation for a given set of R and C. The pulse width range can be varied between 1 μs and 10 ms. The resistor and capacitor timing elements are connected as stated for the Debounce Oscillator R/C input.

Inhibit One-Shot R/C Input

The Inhibit One-Shot R/C Input is a timing input used to disable the Encoder Chip outputs for a period of time after new data has appeared at the outputs and a strobe issued. The inhibit time is necessary to allow the Coded Key inputs to settle out after a keyswitch is depressed. The time slot is adjustable from 1–10 ms ±25%. The recovery time is less than 100 μs. The resistor and capacitor timing elements are connected as stated for the Debounce Oscillator R/C Input.

Delay R/C Input

The Delay R/C Input is a timing input used to determine that valid data is present at the Coded Key Inputs. Valid data must be present continuously for some period of time adjustable between 40 and 80 μs ±25% before the data is accepted as valid data. The resistor and capacitor timing elements are connected as stated for the Debounce Oscillator R/C Input.

Contact Key Outputs

Three contact key outputs designated A–C provide bounce-free non-inverted outputs corresponding to their respective inputs.

Data Outputs

Ten Data Output lines designated B0–B9 are provided. The specific output code related to a given input code and mode must be specified with each reprogramming of the coding mask.

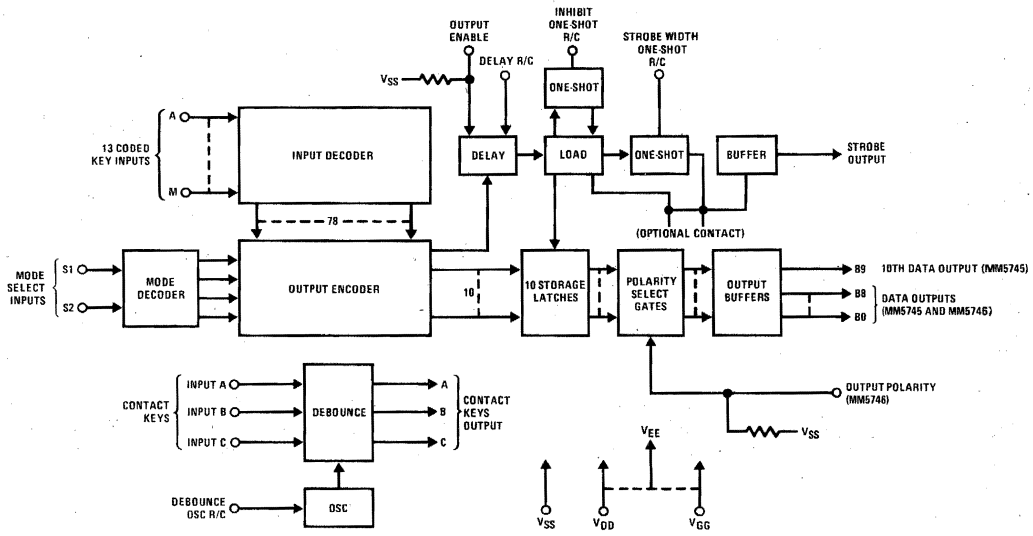


FIGURE 1

functional description (Continued)

Strobe Output

The Strobe Output is used to indicate that new data has just been placed on the Data Output lines.

Data Transfer

Input data, typically in a 2 out of 13 format, is introduced by depressing a keyswitch. The data passes through the input buffers, input inverters, and is decoded into single line codes if the data is valid. There are a maximum of 78 single line codes and these are coded into 41-bit output words. The 41st bit is used to enable the delay R/C timer. Valid input data must be present continuously for typically 60 μs before it is accepted as valid input data and the proper output codes and strobe are generated.

The status of the mode select inputs determines which of the 4 10-bit output codes are selected (first 40 bits). The mode select lines are programmable in binary format and therefore are decoded into single line codes. The output encode in reality has 82 input lines (78 input codes and 4 modes). When a valid input code is present and the mode is selected, the proper 10-bit word is steered through the Mode "OR" Gates and to the inputs of the storage latches. When the proper delay interval has elapsed, the load logic loads the new data into the storage latches.

Both polarities of the 10 data bits are fed to the Polarity Select Gates where the output Data Polarity Input selects the desired polarity output. The selected 10 data bits output the chip through the Output Buffers.

Logic Sequence

The Logic Sequence is not initiated until the successful completion of the delay timing cycle. At the completion of the delay cycle, 3 things happen almost simultaneously. First, a load signal of approximately 2 μs is fed to the storage latches to accept new data. Second, the Strobe Pulse, typically 60 μs wide, is generated. This pulse will not go true until at least 1/2 μs after the data is present at the outputs. Third, the inhibit timing cycle is initiated within 2 μs after the load and strobe inputs are generated and locks out the load and strobe inputs for the duration of the inhibit timing cycle. This insures that only one strobe is generated and no data is changed during the inhibit cycle.

If the input data disappears less than 1/2 μs after the completion of the delay cycle, it is possible that erroneous logic sequencing can take place. The symptoms are new data, but no strobe or no new data, but a strobe is generated.

If the output enable input is held false, no logic sequencing can take place and the chip remains locked up with the existing data statically available at the outputs and no strobes can be generated.

A programming option is available wherein a level strobe can be specified instead of the delayed strobe as described above. In this option, the level strobe goes true at the end of the delay cycle as does the delayed strobe, but is remains true as long as a valid data input signal is present. It is not affected by the inhibit timing cycle. The level strobe responds to the data input lines and is inhibited only by the Output Enable going false.

Debounce Circuits

The debounce circuits utilize a pulse train clock oscillator and shift registers. The input must remain in one state for 2 consecutive clock pulses before it will change the output to that state. The outputs follow the input, in that they are non-inverting.

OPTIONS

The following options are customer specified. (For format information, see Programming Format section).

Input Code

The input code M out of N (typically 2 out of 13) must be specified for each reprogramming of the coding mask.

Mode Select

The Mode Select lines bit pattern must be specified for each mode for each reprogramming of the coding mask. Each mode must be specified whether used or not.

Output Code

The Output Code must be specified for each input code and mode as above.

Strobe

The Delayed Strobe is automatically selected unless the option for the level strobe is selected.

Input Resistors

Each of the 13 inputs and the 2 mode select inputs may have internal resistors (4.5 kΩ ±30%) connected to V_{SS}, V_{DD} or left open.

functional description (Continued)

Programming Format

The MM5745 and MM5746 keyboard encoders are programmed using 4 types of punched data cards whose function and format are explained as follows:

I. Shift Input (Mode Select) Cards

Mode select data is contained in a set of 4 cards which specify the ROM mode to be selected for each of the possible shift input combinations.

SHIFT INPUT CARD FORMAT
(Columns not listed will contain no punches)

Column	Possible Characters	Meaning
1–6	"OPTION"	Shift input–ROM mode assignment to be specified
8	Digits 1–4	Particular shift input
10	= or Blank (Note 5)	Equals, nothing punched
12	Digits 0–3	ROM mode: 0 = Mode 1 1 = Mode 2 2 = Mode 3 3 = Mode 4

II. Device Option Cards

Device option data is contained in a set of 16 cards which specify level or delayed strobe output and establish positive, negative or floating input resistor connections.

DEVICE OPTION CARD FORMAT

Column	Possible Characters	Meaning
1–6	"OPTION"	Device options to be specified
7, 8	Digits 5–20	Involved device inputs and outputs are respectively, A–M, S1, S2 and Delay/Level strobe output
10	= or Blank (Note 5)	Equals, nothing punched
12	Digits 0, 1 or 2	For options 5–19: 0 = No connection 1 = Input resistor tied to V_{DD} 2 = Input resistor tied to V_{SS} For option 20: 0 = Level strobe 1 = Delay strobe

III. Coding Data Cards

ROM coding data is contained in a set of 78 cards with 1 card for each ROM word.

CODING DATA CARD FORMAT

Column	Possible Characters	Meaning
1	Character A	Address character
2, 3	Digits 00–77	ROM word identification (Note 1)
5	Digits 0, 1, 2 or 3 (Note 2)	Input A input code
.		.
.		.
17		Input M input code
20	Digits 0 or 1	IS1 enable gate code (Note 3)
24	Digits 0 or 1	Output 9, mode 1 (Note 4)
.		.
.		.
33		Output 0
36	Digits 0 or 1	Output 9, mode 2 (Note 4)
.		.
.		.
45		Output 0
48	Digits 0 or 1	Output 9, mode 3 (Note 4)
.		.
.		.
57		Output 0
60	Digits 0 or 1	Output 9, mode 4 (Note 4)
.		.
.		.
69		Output 0
71, 72	Digits 00–54	Decimal row sum (total of all 1's in a particular row)

IV. TB Cards

The total of all 1's in the individual columns of data established by the previous Coding Data Cards is stored on 54 TB cards. This allows a cross check of the data.

TB CARD FORMAT

Columns	Possible Characters	Meaning
1,2	TB	TB card identification
3, 4	Digits 00–54	Particular column of data totalled
6	= or Blank	Equals, nothing punched
9, 10	Any value between between 00 and 78	Total of all 1's in that column

Note 1: Words 01 through 09 require leading zeros.

Note 2: A pattern of 0's and 1's describes the input codes. A "2" indicates that neither the original nor the inverted array lines have transistors associated with them, while a "3" means both lines have transistors associated with them.

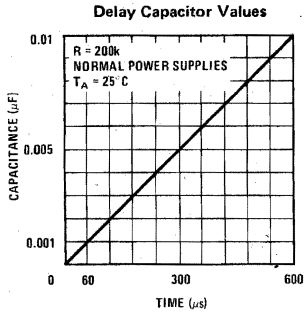
For example, if only 11 inputs are used, use a "2" in the remaining 2. This means only 11 of the 13 gates needs to be checked, thereby increasing yield. If less than 78 inputs are used, a "3" in one of the 13 inputs prevents the input from being used.

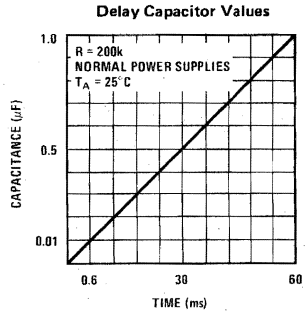
Note 3: A "1" indicates that the IS1 signal will be generated by the word line. A "0" means that IS1 is not generated. Used to block any unused decoded input out of the 78 total.

Note 4: "0" and "1" symbols for the output codes correspond to the logic levels defined for the device outputs.

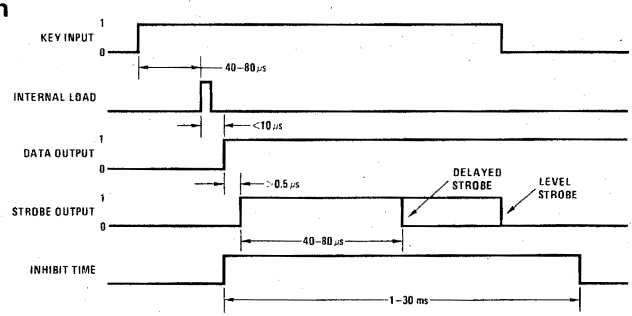
Note 5: If cards were punched on a keypunch machine with character sets other than IBM ϕ29 type, a "BLANK" should be used rather than an "=".

typical performance characteristics





timing diagram



Keyboard Encoder Circuits

MM54C922/MM74C922 16 key encoder
MM54C923/MM74C923 20 key encoder

general description

These CMOS key encoders provide all the necessary logic to fully encode an array of SPST switches. The keyboard scan can be implemented by either an external clock or external capacitor. These encoders also have on-chip pull-up devices which permit switches with up to 50 kΩ on resistance to be used. No diodes in the switch array are needed to eliminate ghost switches. The internal debounce circuit needs only a single external capacitor and can be defeated by omitting the capacitor. A Data Available output goes to a high level when a valid keyboard entry has been made. The Data Available output returns to a low level when the entered key is released, even if another key is depressed. The Data Available will return high to indicate acceptance of the new key after a normal debounce period; this two key roll over is provided between any two switches.

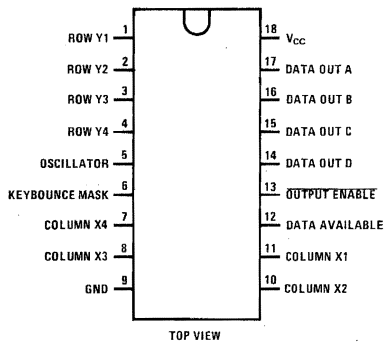
An internal register remembers the last key pressed even after the key is released. The TRI-STATE® outputs provide for easy expansion and bus operation and are LPTTL compatible.

features

- 50 kΩ maximum switch on resistance
- On or off chip clock
- On chip row pull-up devices
- 2 key roll-over
- Keybounce elimination with single capacitor
- Last key register at outputs
- TRI-STATE outputs LPTTL compatible
- Wide supply range 3V to 15V
- Low power consumption

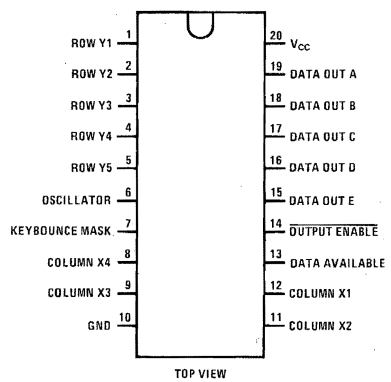
connection diagrams

Dual-In-Line Package



Order Number MM54C922N
or MM74C922N
See Package 20

Dual-In-Line Package



Order Number MM54C923N
or MM74C923N
See Package 20A

absolute maximum ratings

Voltage at Any Pin	V_{CC} − 0.3V to V_{CC} + 0.3V	Package Dissipation	500 mW
Operating Temperature Range		Operating V_{CC} Range	3V to 15V
MM54C922, MM54C923	−55°C to +125°C	V_{CC}	18V
MM74C922, MM74C923	−40°C to +85°C	Lead Temperature (Soldering, 10 seconds)	300°C
Storage Temperature Range	−65°C to +150°C		

dc electrical characteristics Min/max limits apply across temperature range unless otherwise noted

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
CMOS TO CMOS						
V_{T+}	Positive-Going Threshold Voltage at Osc and KBM Inputs	V_{CC} = 5V, $I_{IN} \geq$ 0.7 mA	3	3.6	4.3	V
		V_{CC} = 10V, $I_{IN} \geq$ 1.4 mA	6	6.8	8.6	V
		V_{CC} = 15V, $I_{IN} \geq$ 2.1 mA	9	10	12.9	V
V_{T-}	Negative-Going Threshold Voltage at Osc and KBM Inputs	V_{CC} = 5V, $I_{IN} \geq$ 0.7 mA	0.7	1.4	2	V
		V_{CC} = 10V, $I_{IN} \geq$ 1.4 mA	1.4	3.2	4	V
		V_{CC} = 15V, $I_{IN} \geq$ 2.1 mA	2.1	5	6	V
$V_{IN(1)}$	Logical "1" Input Voltage, Except Osc and KBM Inputs	V_{CC} = 5V,	3.5	4.5		V
		V_{CC} = 10V,	8	9		V
		V_{CC} = 15V,	12.5	13.5		V
$V_{IN(0)}$	Logical "0" Input Voltage, Except Osc and KBM Inputs	V_{CC} = 5V,		0.5	1.5	V
		V_{CC} = 10V,		1	2	V
		V_{CC} = 15V,		1.5	2.5	V
I_{rp}	Row Pull-Up Current at Y1, Y2, Y3, Y4 and Y5 Inputs	V_{CC} = 5V, V_{IN} = 0.1 V_{CC}		−2	−5	μA
		V_{CC} = 10V		−10	−20	μA
		V_{CC} = 15V		−22	−45	μA
$V_{OUT(1)}$	Logical "1" Output Voltage	V_{CC} = 5V, I_O = −10μA	4.5			V
		V_{CC} = 10V, I_O = −10μA	9			V
		V_{CC} = 15V, I_O = −10μA	13.5			V
$V_{OUT(0)}$	Logical "0" Output Voltage	V_{CC} = 5V, I_O = 10μA			0.5	V
		V_{CC} = 10V, I_O = 10μA			1	V
		V_{CC} = 15V, I_O = 10μA			1.5	V
R_{on}	Column "ON" Resistance at X1, X2, X3 and X4 Outputs	V_{CC} = 5V, V_O = 0.5V		500	1400	Ω
		V_{CC} = 10V, V_O = 1V		300	700	Ω
		V_{CC} = 15V, V_O = 1.5V		200	500	Ω
I_{CC}	Supply Current	V_{CC} = 5V, Osc at 0V		0.55	1.1	mA
		V_{CC} = 10V		1.1	1.9	mA
		V_{CC} = 15V		1.7	2.6	mA
$I_{IN(1)}$	Logical "1" Input Current at $\overline{\text{Output Enable}}$	V_{CC} = 15V, V_{IN} = 15V		0.005	1.0	μA
$I_{IN(0)}$	Logical "0" Input Current at $\overline{\text{Output Enable}}$	V_{CC} = 15V, V_{IN} = 0V	−1.0	−0.005		μA
CMOS/LPTTL INTERFACE						
$V_{IN(1)}$	Logical "1" Input Voltage, Except Osc and KBM Inputs	54C, V_{CC} = 4.5V	V_{CC}−1.5			V
		74C, V_{CC} = 4.75V	V_{CC}−1.5			V
$V_{IN(0)}$	Logical "0" Input Voltage, Except Osc and KBM Inputs	54C, V_{CC} = 4.5V			0.8	V
		74C, V_{CC} = 4.75V			0.8	V
$V_{OUT(1)}$	Logical "1" Output Voltage	54C, V_{CC} = 4.5V, I_O = −360μA	2.4			V
		74C, V_{CC} = 4.75V, I_O = −360μA	2.4			V
$V_{OUT(0)}$	Logical "0" Output Voltage	54C, V_{CC} = 4.5V, I_O = −360μA			0.4	V
		74C, V_{CC} = 4.75V, I_O = −360μA			0.4	V

dc electrical characteristics (con't)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
OUTPUT DRIVE (See 54C/74C Family Characteristics Data Sheet)					
I_{SOURCE} Output Source Current (P-Channel)	V_{CC} = 5V, V_{OUT} = 0V, T_A = 25°C	−1.75	−3.3		mA
I_{SOURCE} Output Source Current (P-Channel)	V_{CC} = 10V, V_{OUT} = 0V, T_A = 25°C	−8	−15		mA
I_{SINK} Output Sink Current (N-Channel)	V_{CC} = 5V, V_{OUT} = V_{CC}, T_A = 25°C	1.75	3.6		mA
I_{SINK} Output Sink Current (N-Channel)	V_{CC} = 10V, V_{OUT} = V_{CC}, T_A = 25°C	8	16		mA

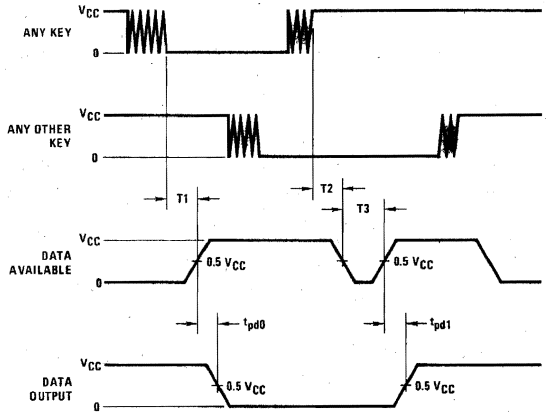
ac electrical characteristics T_A = 25°C

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
t_{pd0},t_{pd1} Propagation Delay Time to Logical "0" or Logical "1" from D.A.	C_L = 50 pF, *(Figure 1)*				
	V_{CC} = 5V		60	150	ns
	V_{CC} = 10V		35	80	ns
	V_{CC} = 15V		25	60	ns
t_{0H},t_{1H} Propagation Delay Time from Logical "0" or Logical "1" into High Impedance State	R_L = 10k, C_L = 5 pF, *(Figure 2)*				
	V_{CC} = 5V R_L = 10k		80	200	ns
	V_{CC} = 10V C_L = 10 pF		65	150	ns
	V_{CC} = 15V		50	110	ns
t_{H0},t_{H1} Propagation Delay Time from High Impedance State to a Logical "0" or Logical "1"	R_L = 10k, C_L = 50 pF, *(Figure 2)*				
	V_{CC} = 5V R_L = 10k		100	250	ns
	V_{CC} = 10V C_L = 50 pF		55	125	ns
	V_{CC} = 15V		40	90	ns
C_{IN} Input Capacitance	Any Input, (Note 2)		5	7.5	pF
C_{OUT} TRI-STATE Output Capacitance	Any Output, (Note 2)		10		pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

switching time waveforms



T1 ≃ T2 ≈ RC, T3 ≈ 0.7 RC where R ≃ 10k and C is external capacitor at KBM input.

FIGURE 1

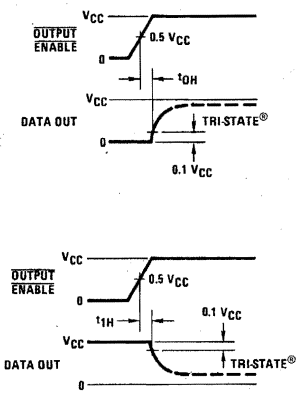
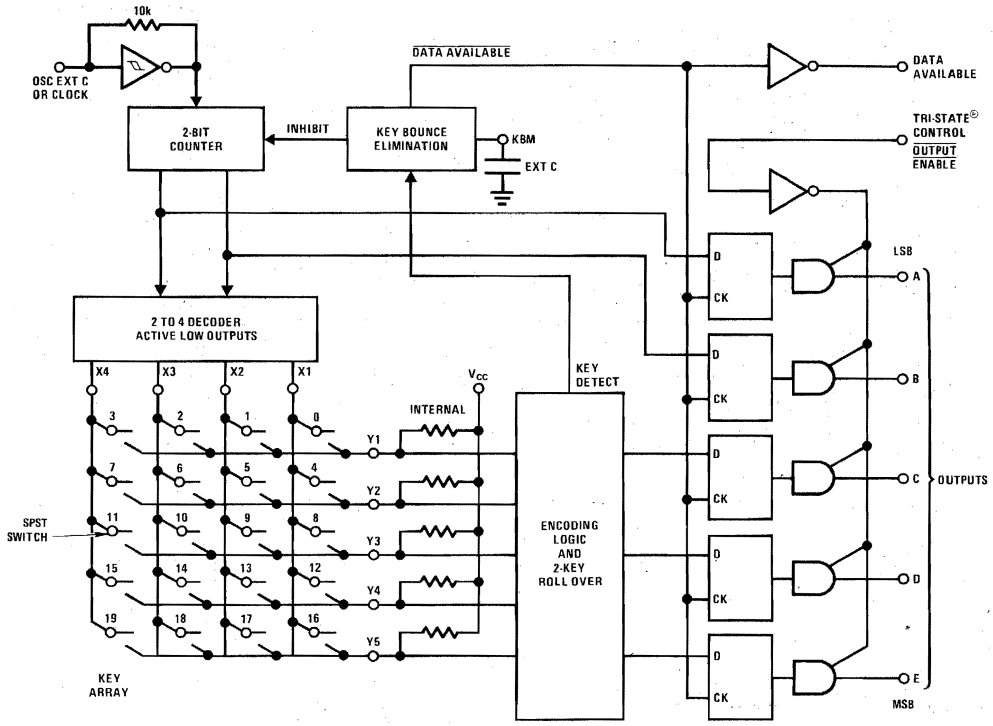


FIGURE 2

block diagram



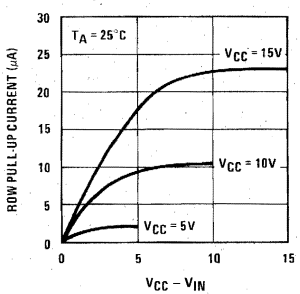
truth table

SWITCH POSITION	0 Y1,X1	1 Y1,X2	2 Y1,X3	3 Y1,X4	4 Y2,X1	5 Y2,X2	6 Y2,X3	7 Y2,X4	8 Y3,X1	9 Y3,X2	10 Y3,X3	11 Y3,X4	12 Y4,X1	13 Y4,X2	14 Y4,X3	15 Y4,X4	16 Y5*,X1	17 Y5*,X2	18 Y5*,X3	19 Y5*,X4
DATA OUT A	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
DATA OUT B	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
DATA OUT C	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1	0	0	0	0
DATA OUT D	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0
DATA OUT E*	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1

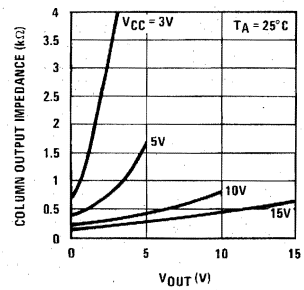
*Omit for MM54C922/MM74C922

typical performance characteristics

Typical I_{rp} vs V_{IN} at Any Y Input



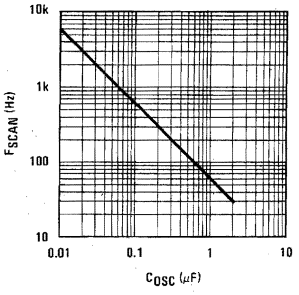
Typical R_{on} vs V_{OUT} at Any X Output



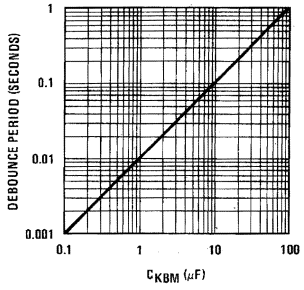
10

typical performance characteristics (con't)

Typical F_{SCAN} vs C_{OSC}

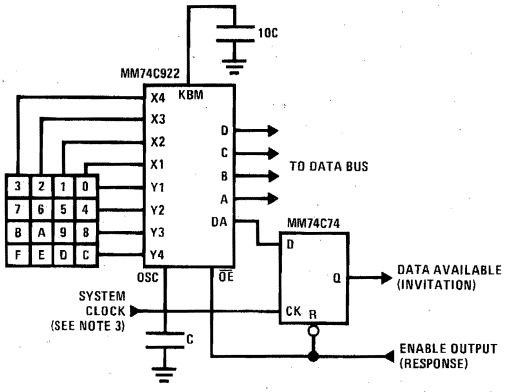


Typical Debounce Period vs C_{KBM}

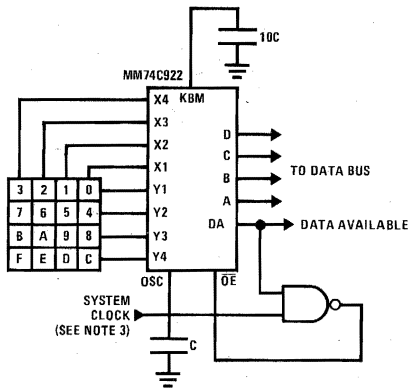


typical applications

Synchronous Handshake (MM74C922)

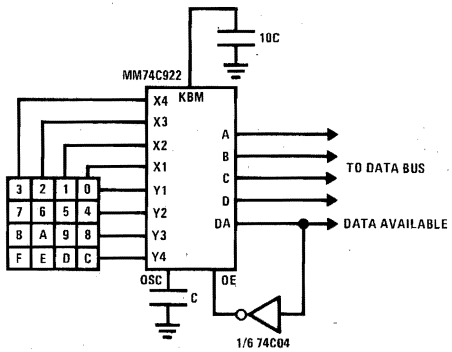


Synchronous Data Entry Onto Bus (MM74C922)



Outputs are enabled when valid entry is made and go into TRI-STATE when key is released.

Asynchronous Data Entry Onto Bus (MM74C922)



Outputs are in TRI-STATE until key is pressed, then data is placed on bus. When key is released, outputs return to TRI-STATE.

Note 3: The keyboard may be synchronously scanned by omitting the capacitor at osc. and driving osc. directly if the system clock rate is lower than 10 kHz.

Keyboard Encoder Circuits

MICROPROCESSOR MATES WITH MOS/LSI KEYBOARD ENCODER

ABSTRACT

This application note is intended to show how to interface a keyboard to the IMP-16 microprocessor for the purpose of text editing. An example which includes suggested hardware and software is presented to illustrate data inputting from the keyboard to the microprocessor. This example can be used either with the IMP-16 chip set or with the IMP-16C/200 or IMP-16C/300 card.

INTRODUCTION

The MM5740 keyboard encoder interfaced to an IMP-16C card microprocessor provides a very cost-effective means of data entry that takes full advantage of the benefits of MOS/LSI technology. The MM5740 is a complete keyboard interface system capable of providing quad mode* 90 key keyboard encoding in a single integrated circuit. This chip detects a key switch closure and translates it into a coded output while providing all of the necessary functions for modern keyboard system design. Data and control outputs are directly compatible with the TTL logic inputs on the IMP-16C. Characters are read from the keyboard into the read/write memory on the IMP-16C card by means of a program contained in PROM's on the card or in external memory. The characters may be reformatted, edited, converted to binary and processed, transferred to a floppy disk or cassette for more permanent recording, or transmitted to a central computer facility. Typical applications include text editing typewriters, alphanumeric CRT display controllers, remote terminal controllers, data entry and recording systems, operators console in man-machine interactive systems, supervisory or process control systems. Further application information is contained in *AN-80 MOS Keyboard Encoding* and *AN-124 IMP-16 Peripheral Interfacing Simplified. Figure 1* is a functional diagram of a keyboard/IMP-16C interface using the LSI keyboard encoder.

INTERFACE CONSIDERATIONS

The Keyboard

Connecting a physical keyboard to the MM5740 will be covered briefly in the following discussion. A more comprehensive treatment is detailed in AN-80, pgs 3 - 4. For this discussion, reference should be made to *Figure 2* which details the pin connections.

The matrix drive (X_1-X_9) and sense (Y_1-Y_{10}) lines are normally connected to each other via the switch matrix. These lines detect contact closure and sense the key that was depressed. The corresponding character is obtained from a read only memory in the MM5740 which has been mask programmed for the desired code. Nine bits are available for each character. Bits 0 to 7 are generally information bits while bits 8 and 9 may be used for parity or special character control. When a valid key is entered the corresponding 9-bit character is stored internally in latches within the MM5740. After a delay of one bit time (one clock period) the data strobe (pin 13) signal will go high, indicating that data is ready and stored in the output latches. This signal alerts the IMP-16C that the character may now be taken. The function of the data strobe control input (pin 14) is to control the resetting of the data strobe once it has been activated. The output enable (pin 15) serves as the TRI-STATE® control for the code data output lines (B_1 to B_9) and is used to control the resetting of the data strobe output.

To minimize response time, the MM5740 is operated in the pulse data strobe mode. The output enable is tied to ground so that the outputs are always enabled. The data strobe is tied directly to the data strobe control. With this connection, a pulse which is one bit time wide will appear on the data strobe line to indicate available data is present. With a 200 kHz clock, one bit time translates into a 5 μs data strobe pulse.

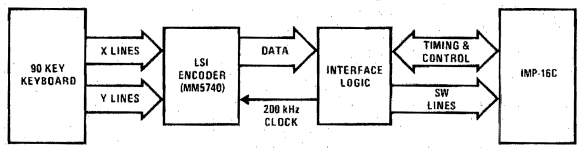


FIGURE 1. Functional Diagram

*Quad mode means the four basic keyboard modes which are; UNSHIFT, SHIFT, CONTROL, SHIFT CONTROL.

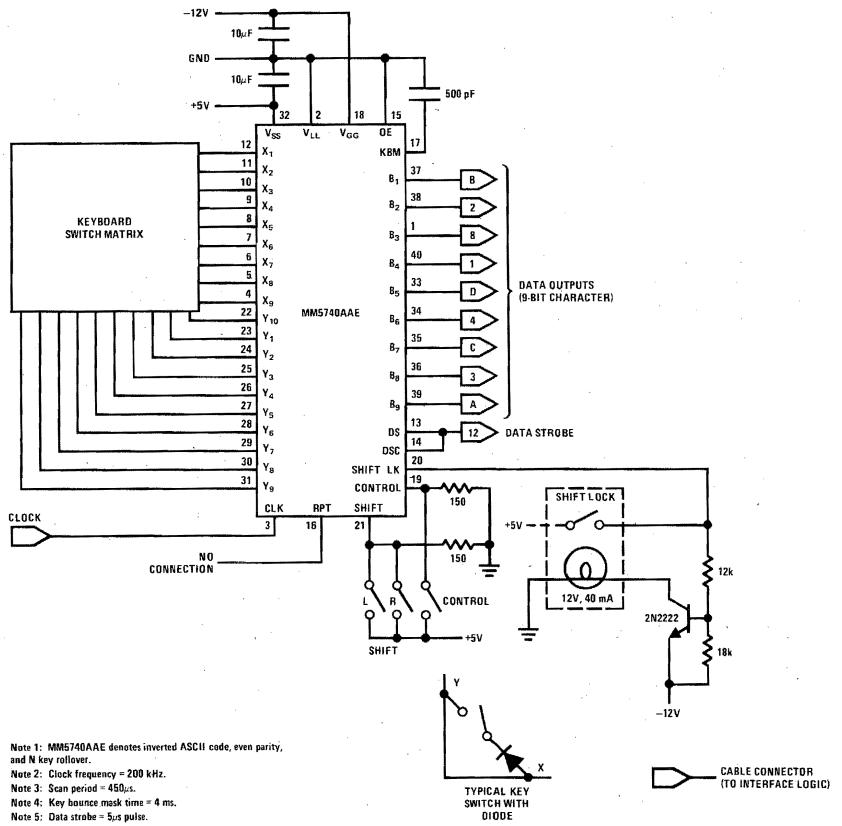


FIGURE 2. MM5740 Pin Connections

In the following sample interface design the MM5740 chip and several discrete components are mounted on a communications keyboard. A cable from the 40 pin connector on the keyboard to an 8 1/2" x 11" interface board provides the physical communications link to the processor. The interface board has space available for components to implement a cassette and CRT interface for text editing applications. Pages of text could be stored as cassette records, called up by the keyboard and displayed on the CRT. Appropriate keyboard commands could be programmed to edit the page. Lines could be inserted, deleted, copied or moved as required. The finished page could be restored on the cassette. *Figure 3* is a schematic diagram of the keyboard interface logic board.

MM5740—IMP-16C INTERFACE

Three instructions are necessary for the IMP-16C to detect that a character is ready for input and to obtain that character. These instructions are given below:

```
LI    3, X '80     ;DEVICE ADDRESS IN AC3
BOC   13, . + 0    ;WAIT FOR CHARACTER READY
RIN   0            ;INPUT CHARACTER INTO AC0
```

The first instruction sets the peripheral device address of the keybaord (X'80) into accumulator 3 (AC3). This is necessary for proper execution of the RIN instruction (AC3 is added to the sign extended displacement field of the RIN instruction and sent to the peripheral over the ADX lines). The address was chosen so as not to be in conflict with any of the IMP-16P peripherals.

The BOC instruction is essentially a test for keyboard character ready. The data strobe output (DSO) from the keyboard (cable connector pin 12) is stored in a set-reset latch built from cross coupled NAND gates (see *Figure 3*). This is because the DSO pulse width is one clock period or 5.0μs and the processor might not detect DSO in the required time. Refer to *Figure 4* for IMP-16C/MM5740 timing. The complement output of the latch ($\overline{Q}$) is connected to jump condition 13 (JC13). The BOC instruction tests for JC13 and branches to the PC relative address specified in the displacement field if the condition is true. Normally JC13 is true; when a key is pressed DSO goes high which forces $\overline{Q}$ low. The jump condition will then be false and the next instruction executed. This next instruction is a RIN 0 which takes the character from the keyboard encoder (B_1 to B_8) into AC0. Thus, this program is in a one-word BOC loop until a key is pressed.

Execution of the RIN instruction causes:

1. The peripheral device address and order code to be placed on the ADX lines at T4 of microcycle 6 (see *Figure 1-3, IMP-16C Application Manual* Supplement 1, pg. 1 - 3. There are eight timing pulses, T1 to T8, each microcycle. The RIN instruction requires 7 of these microcycles).
2. The RDP (Read Peripheral) flag to be pulsed at T2 of microcycle 7. This is used as a peripheral input gating signal.

The peripheral address and order codes on the ADX lines are set into TTL latches on the IMP-16C during RIN microcycle 6. The ADX lines are sent to all peripherals, but only the one whose address is specified

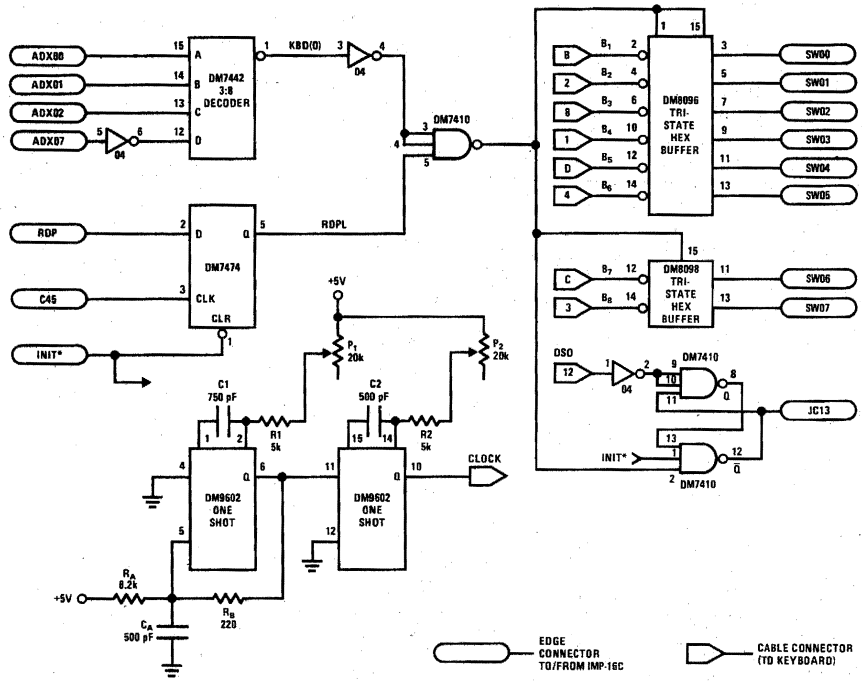


FIGURE 3. Text Editing Keyboard (TEK) Interface Logic for IMP-16C

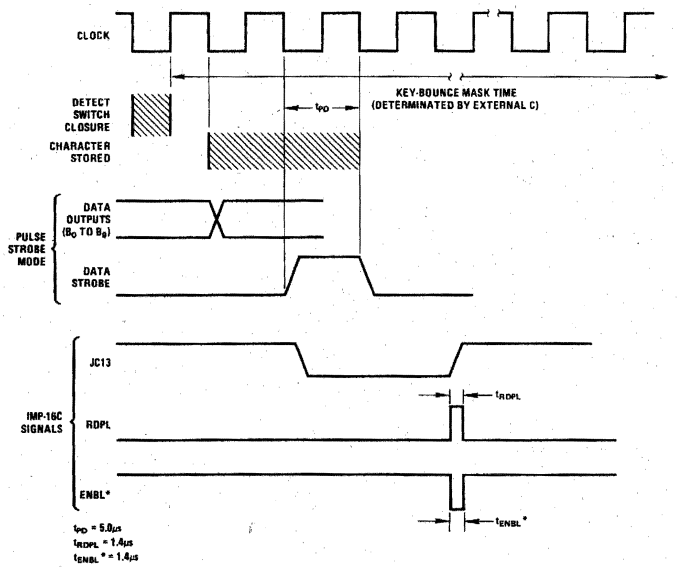


FIGURE 4. MM5740/IMP-C Timing Diagram

will respond. A BCD to binary decoder (DM7442) is used to select one of eight possible order codes. This provides modular expansion capability if new peripherals (keyboards, CRT's, cassettes, printers) are added to the keyboard microprocessor system. The RDP signal is latched (RDPL) on the interface to guarantee that it will be valid at T7 of RIN microcycle 7, when data is taken by the processor. At this time the address and order code is valid and the ENBL signal goes low. This signal enables the TRI-STATE buffers (DM8096, DM8098) which complement the inverted ASCII keyboard data (B_1 to B_8) and place it on the SW bus to the processor. The data is taken by the processor at T7 and transferred into AC0 bits 0 to 7. At this point, one character has been obtained by the processor. The ENBL signal is also used to reset the data strobe latch which makes $\overline{Q}$ high and JC13 true. This reconditions the IMP-16C to be ready for the next character.

The MM5740's clock input (CLK) is provided by a dual one shot (DM9602) connected as an oscillator. A 200 kHz square wave is generated using the logic shown in *Figure 3.*

THE PROGRAM

In addition to the three instructions given, a control program is necessary to pack, store and count characters and insert line delimeters—carriage return (CR) and line feed (LF). A flow chart and coding for the program are given in *Figures 5* and *6*.

A line of text is terminated by a CR or when 72 characters have been entered. The CR—LF is inserted and an address pointer is incremented to designate the start of the next line. At this point, the user may request that the last line or entire message be typed on the teletype using the MESG routine in the TTY 16P PROM. Editing functions such as insert, delete, replace, copy, or move lines could be provided if the information was to be output to a CRT, cassette or floppy disc. Although the keyboard encoder (MM5740) used was mask programmed for inverted ASCII code with even parity, any code could be used.

CONCLUSION

The example below demonstrates a keyboard/microprocessor interface taking full advantage of the benefits of LSI technology—small size, increased reliability, fewer interconnections and much more functional capability per unit cost. These advantages may be exploited in a wide range of man-machine or operator interaction systems.

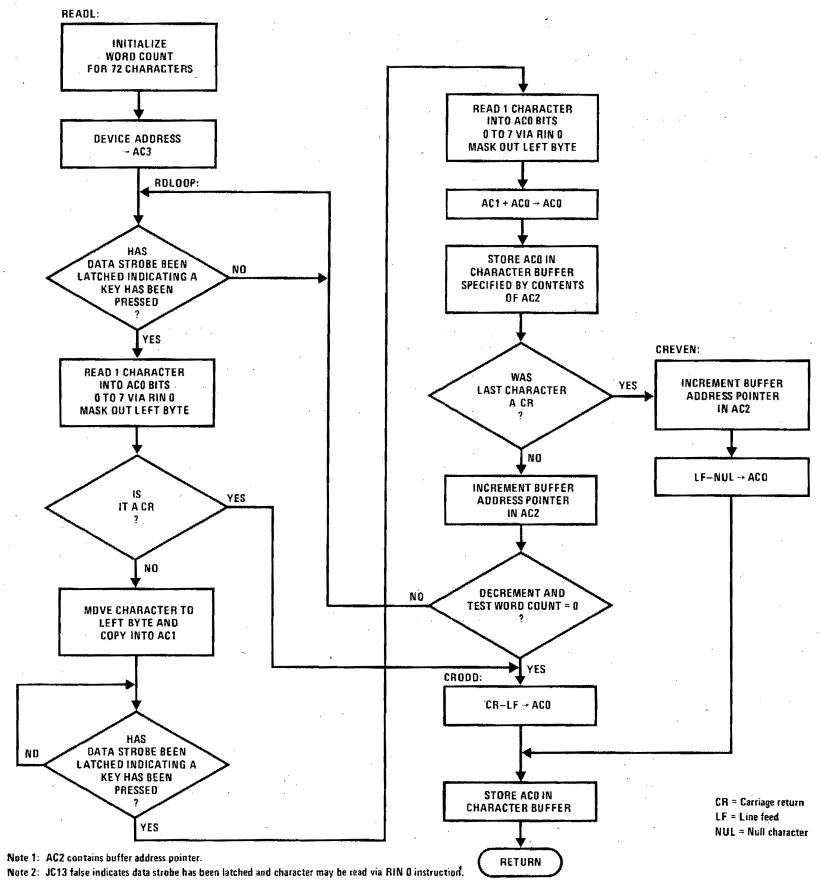


FIGURE 5. Flowchart of Subroutine (READL) that Reads One Line from the Keyboard

```
                                .TITLE TEK
                                .ASECT
                                .=X'700
                        ; MAIN PROGRAM
0700 8914 A  TEK:       LD      2,STADDR        ;INITIALIZE MESG ADDR
0701 A90C A  GO:        ST      2,MADRES
0702 2914 A             JSR     READL           ;READ 1 LINE & STORE
                        ; PUT 1 IN AC0 FOR TTY LINE,0 TO CONTINUE READING,
                        ; 2 TO OUTPUT ALL LINES ON TTY
0703 0000 A             HALT                    ;ENTER 0/1/2 IN AC0
0704 1305 A             BOC     3,OUTL          ;BIT0 AC0=1 OUT LINE
0705 1402 A             BOC     4,OUTM          ;BIT1 AC0=1 OUT MESAG
                        ;  CONTINUE ENTERING NEXT LINE BY DEFAULT
0706 4A01 A             AISZ    2,1             ;INCR ADDRESS PTR
0707 21F9 A             JMP     GO              ;CONTINUE
                        ;  OUTPUT ENTIRE MESSAGE ON TTY
0708 850C A  OUTM:      LD      1,STADDR        ;SETUP MESG STARTING
0709 A504 A             ST      1,MADRES        ;    ADDRESS
                        ; ENTER 0 AS LAST WORD FOR MESG ROUTINE IN TTY16P
                        ;  OUTPUT LINE OR MESSAGE
070A 4A01 A  OUTL:      AISZ    2,1             ;INCR ADDRESS
070B 4C00 A             LI      0,0
070C A200 A             ST      0,(2)
                        ; OUTPUT ON TTY USING MESG SR IN TTY16P PROM
070D 2D08 A             JSR     @MESG           ;OUTPUT ON TTY
070F        MADRES:     .=.+1                   ;MESSAGE ADDRESS
070F 21F1 A             JMP     GO              ;READ NEXT LINE
                        ;
                        ; DATA AREA
0711        WDCNT:      .=.+1                   ;WORD COUNT FOR KBD
0711 00FF A H00FF:      .WORD   X'00FF          ;MASK RT WD
0712 008D A CR:         .WORD   X'008D          ;CR W PARITY BIT
0713 0D0A A CRLF:       .WORD   X'0D0A          ;'CR-LF'
0714 0A00 A LFNULL:     .WORD   X'0A00          ;'LF-NUL'
0715 1000 A STADDR:     .WORD   X'1000          ;ST ADDRESS OF MESG
0716 7EC3 A MESG:       .WORD   X'7EC3          ;MESG SR ADDR TTY16P
                        ; READ 1 LINE FROM KEYBOARD & STORE IN 36 WD BUFFER
                        ; STARTING BUFFER ADDRESS IN AC2
                        ; CHARS ARE READ,PACKED & STORED
                        ; CR IS TERMINAING CHAR.  CR LF AT END OF LINE
                        ;  JC13 FOR DATA STROBE OUTPUT WHEN KEY IS PRESSED
0717 4C24 A  READL:     LI      0,36            ;WORD COUNT
0718 A1F7 A             ST      0,WDCNT
0719 4F80 A             LI      3,X'80          ;DEVICE ADDRESS
071A 1DFF A  RDLOOP:    BOC     13,.+0          ;WAIT FOR DATA STROBE
071B 0400 A             RIN     0               ;READ 1 CHAR INTO AC0
071C 61F4 A             AND     0,H00FF         ;MASK OUT LEFT BYTE
071D F1F4 A             SKNE    0,CR            ;IS IT A 'CR'
071E 210D A             JMP     CRODD
071F 5C08 A             SHL     0,8             ;MOVE TO LEFT BYTE
0720 3181 A             RCPY    0,1
0721 1DFF A             BOC     13,.+0          ;WAIT FOR DATA STROBE
0722 0400 A             RIN     0               ;READ 1 CHAR INTO AC0
0723 61ED A             AND     0,H00FF         ;MASK OUT LEFT BYTE
0724 3400 A             RADD    1,0             ;2 PACKED CHARS
0725 A200 A             ST      0,(2)           ;STORE IN BUFFER
0726 61EA A             AND     0,H00FF         ;WAS LAST CHAR A CR
0727 F1EA A             SKNE    0,CR
0728 2106 A             JMP     CREVEN
0729 4A01 A             AISZ    2,1             ;INCR ADDR POINTER
072A 7DE5 A             DSZ     WDCNT           ;DECR & TEST WD COUNT
072B 21EE A             JMP     RDLOOP
                        ;.....................................................
                        ; ENTER CR-LF AS LAST WORD
```

FIGURE 6. Coding for Text Editing Keyboard (TEK)

```
65 072C 81E6 A  CRODD:  LD      0,CRLF          ;CR/LINE FEED CHARS
66 072D A200 A          ST      0,(2)           ;STORE IN BUFFER
67 072E 0200 R          RTS     0
68                ; ENTER LF-NUL AS LAST WORD
69 072F 4A01 A  CREVEN: AISZ    2,1              ;INCR ADDRESS PTR
70 0730 81E3 A          LD      0,LFNULL        ;LINE FEED/NULL CHARS
71 0731 21FB A          JMP     CRODD+1
72                ;
73                ;  MESSAGE BUFFER
74                ;  EACH LINE CONTAINS A MAXIMUM OF 72 PACKED CHARS
75                ;  AND A CR-LF
76      1000              .=X'1000
77      0700              .END    TEK

CR      0712  A
CREVEN  072F  A
CRLF    0713  A
CRODD   072C  A
GO      0701  A
H00FF   0711  A
LFNULL  0714  A
MADRES  070E  A
MESG    0716  A
OUTL    070A  A
OUTM    0708  A
RDLOOP  071A  A
READL   0717  A
STADDR  0715  A
TEK     0700  A
WDCNT   0710  A
NO ERROR LINES
SOURCE CK. = AE1A
```

FIGURE 6. Coding for Text Editing Keyboard (TEK) (Continued)

Keyboard Encoder Circuits

MOS ENCODER PLUS PROM YIELD QUICK TURNAROUND KEYBOARD SYSTEMS*

INTRODUCTION

Most modern keyboard designs employ MOS/LSI keyboard encoder IC's to implement all the necessary electronic functions. The key codes specified by the customer are programmed into a read only memory which is an inherent part of the encoder. Although some common encoder formats are available off the shelf, such as ASR33 teletype (MM5740AAE or MM5740AAF), there are many instances where variations of common formats are needed. Since these formats are mask programmed into the keyboard encoder, there is a certain amount of lead time (approximately 12 weeks) before a customer receives his final circuit.

By using a binary coded keyboard encoder in conjunction with a programmable read only memory, customers can build prototype keyboard systems or fill small volume orders in minimum time. This approach keeps all the encoding electronics and timing the same as in the final system, so that a minimum of redesign is necessary to configure the actual final version. This is done when the keyboard encoder with the final mask programmed key codes is received. In addition, the usefulness of being able to reassign key codes quickly in the PROM makes system debugging and alteration an easy task.

The basic configuration for this implementation is shown in the simplified block diagram of *Figure 1.* The key switches and all timing signals are configured in the normal manner. The keyboard encoder chip will emit binary codes for each valid keyswitch closure. These binary outputs are used as addresses for the PROM which is programmed with the desired actual code for each keyswitch. Each key closure is transformed first to an address by the encoder and then to the final code by the PROM. In this manner, a general design is possible, with the only variable being the contents of the PROM which is easily and quickly programmed. When changes are necessary, the PROM may be erased and reprogrammed quickly making it an easy task to finalize design alterations.

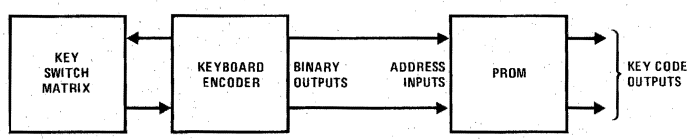


FIGURE 1. Simplified Block Diagram

***REFERENCE:** AN-80 MOS Keyboard Encoding by Dom Richiuso

KEYBOARD IMPLEMENTATION

A typical implementation of this approach is shown in *Figure 2.* The encoder employs a dynamic scanning technique to identify key closures. Each keyswitch is defined by a particular X drive line and Y sense line of the encoder. In addition to the basic operation of translating a switch closure to a coded output, the MM5740

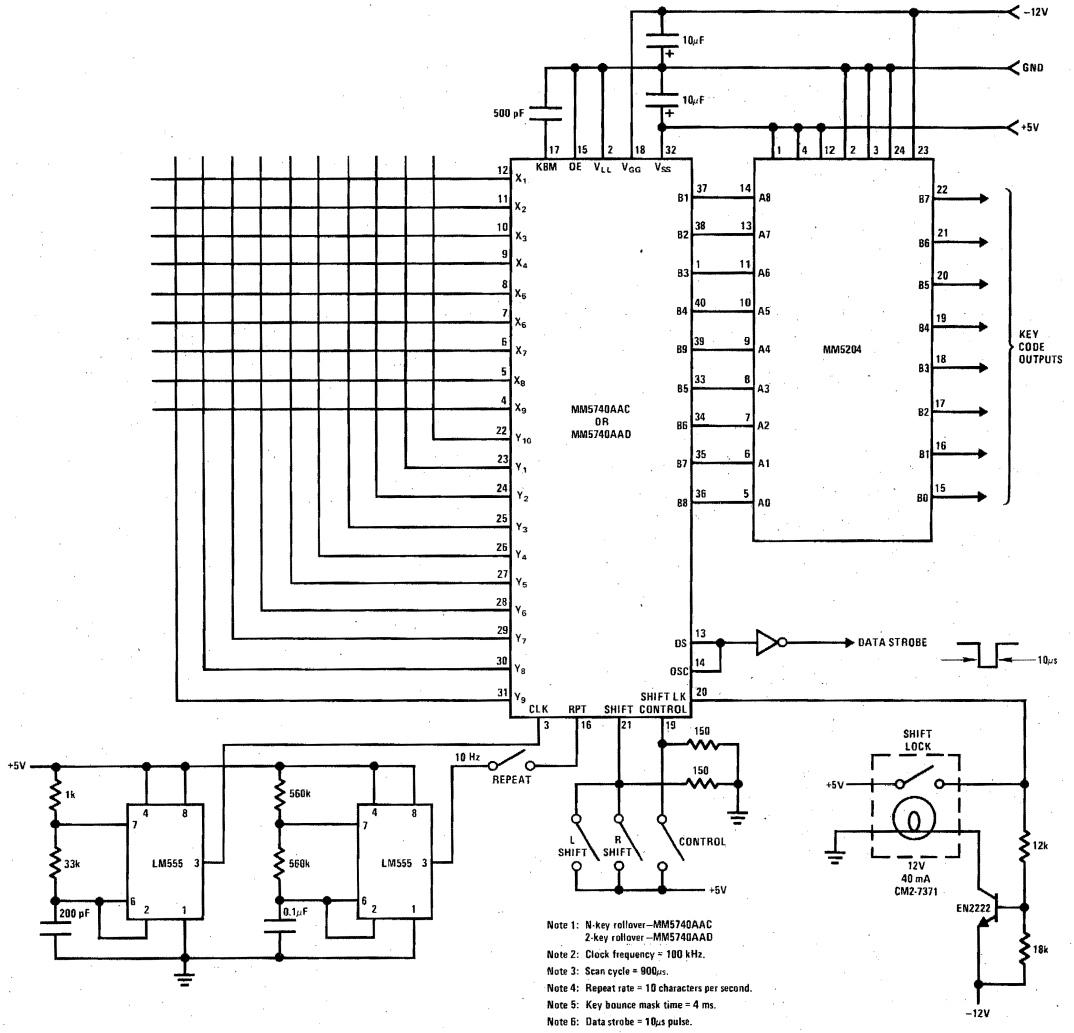


FIGURE 2. Typical Keyboard System

provides all the functions necessary for modern keyboard system design. This includes all the logic necessary for key validation, 2-key or N-key rollover, bounce masking, mode selection and strobe generation. Table I illustrates the relationship between keyswitch matrix position, key mode and the binary coded outputs of the MM5740 AAC or AAD encoder. The AAC version provides for N-key rollover while the AAD is a 2-key rollover encoder. Since there are nine X lines, ten Y lines and four modes, 360 nine-bit codes are possible.

In the general application using 90 four mode keys, a 4k PROM (MM5204) should be used. If less than 64 four-mode keys are all that is required, a 2k PROM (MM5203) may be substituted. In this case, the most significant bit (B1) from the encoder is dropped and Table I addresses would go from 0–255. When programming the PROM, it should be noted that the MM5740 uses a bit paired coding system. Any particular key will have 5 common bits (B1, B2, B3, B4, B9) and 4 variable bits (B5, B6, B7, B8) which may change when going from one mode to another. In addition, encoder coding is specified in terms of negative logic so that it may be necessary to complement positive logic PROM contents when ordering encoder masks.

By careful PC board layout, the encoder/PROM prototyping system can utilize the same PC board as the final system with the PROM removed. This can be accomplished by arranging the traces so that it is possible to provide jumpers from the encoder outputs to the PROM outputs. Utilizing this approach allows for a minimum of tooling, parts counts and quick turnaround time for new designs.

TABLE I. Encoder/PROM Mapping

	KEY POSITION		MODE	ADDRESSES (ENCODER OUTPUT)									KEY CODE OUTPUTS (PROM CONTENTS)							
	X	Y		B1	B2	B3	B4	B9	B5	B6	B7	B8	B7	B6	B5	B4	B3	B2	B1	B0
KEY 1	1	1	Unshift	0	0	0	0	0	0	0	0	0								
	1	1	Shift	0	0	0	0	0	0	0	0	1								
	1	1	Control	0	0	0	0	0	0	0	1	0								
	1	1	Shift Control	0	0	0	0	0	0	0	1	1								
	1	2	Unshift	0	0	0	0	0	0	1	0	0								
	1	2	Shift	0	0	0	0	0	0	1	0	1								
	1	2	Control	0	0	0	0	0	0	1	1	0								
	1	2	Shift Control	0	0	0	0	0	0	1	1	1								
	.		.					.					USER DEFINED KEY CODES							
	.		.					.												
	.		.					.												
KEY 90	9	10	Unshift	1	0	1	1	0	0	1	0	0								
	9	10	Shift	1	0	1	1	0	0	1	0	1								
	9	10	Control	1	0	1	1	0	0	1	1	0								
	9	10	Shift Control	1	0	1	1	0	0	1	1	1								

*Encoder outputs are listed in positive true logic notation.

TABLE II. Truth Table
MM5740/AAC or MM5740/AAD

MATRIX ADDRESS		COMMON					UNSHIFT				SHIFT				CONTROL				SHIFT CONTROL			
		B1	B2	B3	B4	B9	B5	B6	B7	B8	B5	B6	B7	B8	B5	B6	B7	B8	B5	B6	B7	B8
1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	0	1	1	1	0	0
1	2	1	1	1	1	1	1	0	1	1	1	0	1	0	1	0	0	1	1	0	0	0
1	3	1	1	1	1	1	0	1	1	1	0	1	1	0	0	1	0	1	0	1	0	0
1	4	1	1	1	1	1	0	0	1	1	0	0	1	0	0	0	0	1	0	0	0	0
1	5	1	1	1	1	0	1	1	1	1	1	1	1	0	1	1	0	1	1	1	0	0
1	6	1	1	1	1	0	1	0	1	1	1	0	1	0	1	0	0	1	1	0	0	0
1	7	1	1	1	1	0	0	1	1	1	0	1	1	0	0	1	0	1	0	1	0	0
1	8	1	1	1	1	0	0	0	1	1	0	0	1	0	0	0	0	1	0	0	0	0
1	9	1	1	1	0	1	1	1	1	1	1	1	1	0	1	1	0	1	1	1	0	0
1	10	1	1	1	0	1	1	0	1	1	1	0	1	0	1	0	0	1	1	0	0	0
2	1	1	1	1	0	1	0	1	1	1	0	1	1	0	0	1	0	1	0	1	0	0
2	2	1	1	1	0	1	0	0	1	1	0	0	1	0	0	0	0	1	0	0	0	0
2	3	1	1	1	0	0	1	1	1	1	1	1	1	0	1	1	0	1	1	1	0	0
2	4	1	1	1	0	0	1	0	1	1	1	0	1	0	1	0	0	1	1	0	0	0
2	5	1	1	1	0	0	0	1	1	1	0	1	1	0	0	1	0	1	0	1	0	0
2	6	1	1	1	0	0	0	0	1	1	0	0	1	0	0	0	0	1	0	0	0	0
2	7	1	1	0	1	1	1	1	1	1	1	1	1	0	1	1	0	1	1	1	0	0
2	8	1	1	0	1	1	1	0	1	1	1	0	1	0	1	0	0	1	1	0	0	0
2	9	1	1	0	1	1	0	1	1	1	0	1	1	0	0	1	0	1	0	1	0	0
2	10	1	1	0	1	1	0	0	1	1	0	0	1	0	0	0	0	1	0	0	0	0
3	1	1	1	0	1	0	1	1	1	1	1	1	1	0	1	1	0	1	1	1	0	0
3	2	1	1	0	1	0	1	0	1	1	1	0	1	0	1	0	0	1	1	0	0	0
3	3	1	1	0	1	0	0	1	1	1	0	1	1	0	0	1	0	1	0	1	0	0
3	4	1	1	0	1	0	0	0	1	1	0	0	1	0	0	0	0	1	0	0	0	0
3	5	1	1	0	0	1	1	1	1	1	1	1	1	0	1	1	0	1	1	1	0	0
3	6	1	1	0	0	1	1	0	1	1	1	0	1	0	1	0	0	1	1	0	0	0
3	7	1	1	0	0	1	0	1	1	1	0	1	1	0	0	1	0	1	0	1	0	0
3	8	1	1	0	0	1	0	0	1	1	0	0	1	0	0	0	0	1	0	0	0	0
3	9	1	1	0	0	0	1	1	1	1	1	1	1	0	1	1	0	1	1	1	0	0
3	10	1	1	0	0	0	1	0	1	1	1	0	1	0	1	0	0	1	1	0	0	0
4	1	1	1	0	0	0	0	1	1	1	0	1	1	0	0	1	0	1	0	1	0	0
4	2	1	1	0	0	0	0	0	1	1	0	0	1	0	0	0	0	1	0	0	0	0
4	3	1	0	1	1	1	1	1	1	1	1	1	1	0	1	1	0	1	1	1	0	0
4	4	1	0	1	1	1	1	0	1	1	1	0	1	0	1	0	0	1	1	0	0	0
4	5	1	0	1	1	1	0	1	1	1	0	1	1	0	0	1	0	1	0	1	0	0
4	6	1	0	1	1	1	0	0	1	1	0	0	1	0	0	0	0	1	0	0	0	0
4	7	1	0	1	1	0	1	1	1	1	1	1	1	0	1	1	0	1	1	1	0	0
4	8	1	0	1	1	0	1	0	1	1	1	0	1	0	1	0	0	1	1	0	0	0
4	9	1	0	1	1	0	0	1	1	1	0	1	1	0	0	1	0	1	0	1	0	0
4	10	1	0	1	1	0	0	0	1	1	0	0	1	0	0	0	0	1	0	0	0	0
5	1	1	0	1	0	1	1	1	1	1	1	1	1	0	1	1	0	1	1	1	0	0
5	2	1	0	1	0	1	1	0	1	1	1	0	1	0	1	0	0	1	1	0	0	0
5	3	1	0	1	0	1	0	1	1	1	0	1	1	0	0	1	0	1	0	1	0	0
5	4	1	0	1	0	1	0	0	1	1	0	0	1	0	0	0	0	1	0	0	0	0
5	5	1	0	1	0	0	1	1	1	1	1	1	1	0	1	1	0	1	1	1	0	0
5	6	1	0	1	0	0	1	0	1	1	1	0	1	0	1	0	0	1	1	0	0	0
5	7	1	0	1	0	0	0	1	1	1	0	1	1	0	0	1	0	1	0	1	0	0
5	8	1	0	1	0	0	0	0	1	1	0	0	1	0	0	0	0	1	0	0	0	0
5	9	1	0	0	1	1	1	1	1	1	1	1	1	0	1	1	0	1	1	1	0	0
5	10	1	0	0	1	1	1	0	1	1	1	0	1	0	1	0	0	1	1	0	0	0
6	1	1	0	0	1	1	0	1	1	1	0	1	1	0	0	1	0	1	0	1	0	0
6	2	1	0	0	1	1	0	0	1	1	0	0	1	0	0	0	0	1	0	0	0	0
6	3	1	0	0	1	0	1	1	1	1	1	1	1	0	1	1	0	1	1	1	0	0
6	4	1	0	0	1	0	1	0	1	1	1	0	1	0	1	0	0	1	1	0	0	0
6	5	1	0	0	1	0	0	1	1	1	0	1	1	0	0	1	0	1	0	1	0	0
6	6	1	0	0	1	0	0	0	1	1	0	0	1	0	0	0	0	1	0	0	0	0
6	7	1	0	0	0	1	1	1	1	1	1	1	1	0	1	1	0	1	1	1	0	0
6	8	1	0	0	0	1	1	0	1	1	1	0	1	0	1	0	0	1	1	0	0	0
6	9	1	0	0	0	1	0	1	1	1	0	1	1	0	0	1	0	1	0	1	0	0
6	10	1	0	0	0	1	0	0	1	1	0	0	1	0	0	0	0	1	0	0	0	0
7	1	1	0	0	0	0	1	1	1	1	1	1	1	0	1	1	0	1	1	1	0	0
7	2	1	0	0	0	0	1	0	1	1	1	0	1	0	1	0	0	1	1	0	0	0
7	3	1	0	0	0	0	0	1	1	1	0	1	1	0	0	1	0	1	0	1	0	0
7	4	1	0	0	0	0	0	0	1	1	0	0	1	0	0	0	0	1	0	0	0	0
7	5	0	1	1	1	1	1	1	1	1	1	1	1	0	1	1	0	1	1	1	0	0
7	6	0	1	1	1	1	1	0	1	1	1	0	1	0	1	0	0	1	1	0	0	0
7	7	0	1	1	1	1	0	1	1	1	0	1	1	0	0	1	0	1	0	1	0	0
7	8	0	1	1	1	1	0	0	1	1	0	0	1	0	0	0	0	1	0	0	0	0
7	9	0	1	1	1	0	1	1	1	1	1	1	1	0	1	1	0	1	1	1	0	0
7	10	0	1	1	1	0	1	0	1	1	1	0	1	0	1	0	0	1	1	0	0	0
8	1	0	1	1	1	0	0	1	1	1	0	1	1	0	0	1	0	1	0	1	0	0
8	2	0	1	1	1	0	0	0	1	1	0	0	1	0	0	0	0	1	0	0	0	0
8	3	0	1	1	0	1	1	1	1	1	1	1	1	0	1	1	0	1	1	1	0	0
8	4	0	1	1	0	1	1	0	1	1	1	0	1	0	1	0	0	1	1	0	0	0
8	5	0	1	1	0	1	0	1	1	1	0	1	1	0	0	1	0	1	0	1	0	0
8	6	0	1	1	0	1	0	0	1	1	0	0	1	0	0	0	0	1	0	0	0	0
8	7	0	1	1	0	0	1	1	1	1	1	1	1	0	1	1	0	1	1	1	0	0
8	8	0	1	1	0	0	1	0	1	1	1	0	1	0	1	0	0	1	1	0	0	0
8	9	0	1	1	0	0	0	1	1	1	0	1	1	0	0	1	0	1	0	1	0	0
8	10	0	1	1	0	0	0	0	1	1	0	0	1	0	0	0	0	1	0	0	0	0
9	1	0	1	0	1	1	1	1	1	1	1	1	1	0	1	1	0	1	1	1	0	0
9	2	0	1	0	1	1	1	0	1	1	1	0	1	0	1	0	0	1	1	0	0	0
9	3	0	1	0	1	1	0	1	1	1	0	1	1	0	0	1	0	1	0	1	0	0
9	4	0	1	0	1	1	0	0	1	1	0	0	1	0	0	0	0	1	0	0	0	0
9	5	0	1	0	1	0	1	1	1	1	1	1	1	0	1	1	0	1	1	1	0	0
9	6	0	1	0	1	0	1	0	1	1	1	0	1	0	1	0	0	1	1	0	0	0
9	7	0	1	0	1	0	0	1	1	1	0	1	1	0	0	1	0	1	0	1	0	0
9	8	0	1	0	1	0	0	0	1	1	0	0	1	0	0	0	0	1	0	0	0	0
9	9	0	1	0	0	1	1	1	1	1	1	1	1	0	1	1	0	1	1	1	0	0
9	10	0	1	0	0	1	1	0	1	1	1	0	1	0	1	0	0	1	1	0	0	0

*NEGATIVE LOGIC NOTATION "1" = –, "0" = +